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On-chip interconnect: design and modeling

State of the art in interconnect extraction is mostly RC. Post layout extraction for high frequency design
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Optimization with Recourse of Analog Circuits including Layout Extraction, Capacitance of RC Interconnect, for VLSI Interconnect

Vlsi - university of michigan

IEEE Transactions on Very Large Scale Integration Inhee Lee, Qing Manycore Interconnect Fabric,"
IEEE Symposium on VLSI

Optem: submicron ic tools - interconnect modeling,

IC package interconnect modeling; and general pre-layout software tool used for layout-to-circuit device and interconnect RC extraction of

A reliable quick parasitic capacitance extraction

A reliable quick parasitic capacitance extraction tool for the physical layer in communication (VLSI) form the basis for Zhu QK (2002) Interconnect RC and

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Smartextract: parasite extraction

interconnect RC is a significant portion of circuit performance, In a typical design flow, parasitic extraction and timing analysis are two independent steps.

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Qing K. Zhu and Paige Kolze MOS Layout CHESS: A Comprehensive Tool for CDFG Extraction and Synthesis

Postlayout eda tools lock onto full-chip

Postlayout EDA tools lock onto and a final performance simulation that uses interconnect RC Simon, "Technical White Paper on RC Extraction," Epic Design

Parasitic extraction - wikipedia, the free

In electronic design automation, parasitic extraction is calculation of the parasitic effects in both the designed devices and the required wiring interconnects of an

Interconnect analysis - icscape inc

Accelerate Design Closure. in-design, pre-LVS and post-extraction parasitic analysis. Handles large RC networks like power mesh; Interconnect calculator for

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Beol variability and impact on rc extraction - dac

BEOL Variability and Impact on RC Extraction Nagaraj NS, Design, Performance, process realities and interconnect extraction [1].

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High-Speed Clock Network Design is a collection of design Power Distribution Network Design for VLSI Qing K Zhu Inbunden Layout guidelines. 5

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We focus on interconnect design, extraction, and 2D/3D substrate and interconnect RC extraction for detailed analysis of crosstalk and delay effects at the cell

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Lasca- interconnect parasitic extraction tool for

LASCA-interconnect parasitic extraction tool for deep-submicron IC design Full Text Sign RC models; VLSI; layout extraction; polygon distribution;

Buffered steiner tree construction with wire

This paper presents an efficient algorithm for buffered Steiner tree construction with "Interconnect Layout extraction of interconnect parasitics in VLSI

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when compared to traditional layout extraction (2D PARASITIC EXTRACTION Interconnect capacitance in each node in a model for RC extraction, e.g, distributed

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Rc extraction : top level interconnect only |

Hi, I am trying to do top level interconnect extraction using Calibre RCX. This is a mixed signal design (most sub-blocks using analog flow + one digital block which

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interconnect and substrate extraction software tool for techniques are used to accurately and efficiently extract these RC values from the layout.

Pillage, "rice: rapid interconnect circuit

by Qing Zhu, Wayne W.M. Dai, Joe G. Xi The clock network can exhibit distributed RC and lossy Our models comprehend key interconnect circuit and layout

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of the IFIP/IEEE International Conference on Very Large Scale Integration Q. Zhu, K. Vaidyanathan, O. L. Pileggi, RC(L)Interconnect Sizing With Second

Rc book

The HDR Book: Unlocking the Pros Advanced Field-Solver Techniques for RC Extraction of Integrated Circuits By Wenjian Yu, Interconnect RC and Layout

2007 ic/cad contest problem b3 interconnect

2007 IC/CAD Contest Problem B3 Interconnect Parasitic RC Extraction Source: Cadence Design Systems, Inc. 1. Introduction In submicron processes, signal delay due

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